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RESEARCH ARTICLE

Materials Science

Mechanically exfoliated graphene from Sri Lankan vein graphite for field effect transistor application

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Abstract: In this work, a single layer of graphene was exfoliated from Sri Lankan vein graphite obtained from the Kahatagaha graphite mines, and field effect transistors (FETs) were fabricated to study their electronic properties. Graphite pieces were carefully examined, and a small piece of graphite was separated with possible large graphene sheets. A simple Scotch tape technique was used to transfer graphene from the selected graphite pieces onto a 300 nm SiO_2 coated Si (SiO_2/Si) substrate for FET fabrication. The thickness and the uniformity of the graphene layers were tested using atomic force microscopy (AFM). The thickness of the transferred single layer graphene was confirmed to be 0.4 nm. The AFM images also confirmed the presence of double layer graphene with thickness of 0.9 nm. FETs were fabricated by creating electrical contacts using successive thermal evaporation of chrome and gold on the transferred graphene layers with a channel length of 5 µm. Results showed that the graphene FETs showed an ambipolar current response with a positive Dirac voltage. The calculated average electron and hole mobility in the graphene channel were 252 (±57) and 592 (±125) $cm^2V^{-1}s^{-1}$ respectively. The positive Dirac voltage could be attributed to the sulphur content in the graphite obtained from Kahatagaha graphite mines. Our studies suggests that the Sri Lankan graphite can be used as a raw material for graphene exfoliation and device application.

Keywords: Field effect transistor, graphene, graphite, Kahatagaha graphite mine, mobility, Sri Lanka.

INTRODUCTION

Graphene is a single atomic layer of graphite and, consists of carbon atoms which are arranged in a two-dimensional honeycomb lattice (Geim & Novoselov, 2007). Graphene has unique mechanical and electronic properties, by having σ bonds of 1.46 Å and a 2.46 Å lattice parameter. It shows zero gap semiconductor properties with charge carrier mobility greater than 2×10^5 cm^2/V s and thermal conductivity greater than 3000 W/m K (Li *et al*., 2014). The field effect transistor (FET) plays a leading role in different electronic applications. The graphene FET consists of single or multiple layers of graphene or a thin film made up of graphene flakes as a channel (Novoselov *et al*., 2004; Geim & Novoselov, 2007; Schedin *et al*., 2007). Due to the zero bandgap of graphene, typical graphene FETs exhibit ambipolar behavior (Reddy *et al*., 2011). A graphene based FET has a high reactivity to electrical perturbation and high carrier mobility. Due to these properties, graphene FET devices have been used in various applications including biosensors (Murugathas *et al*., 2020).

Graphene was first identified and recognized in 2004, by Geim and Novoselov (Novoselov *et al*., 2004). A small amount of graphene were obtained by peeling the layers apart from the highly oriented pyrolytic graphite (HOPG) crystals using Scotch tape. In 2010 Geim and Novosolv won the Nobel prize for the discovery and characterization of graphene sheets (Novoselov *et al*., 2004). Thereafter, several techniques have been established for graphene synthesis. They are mechanical exfoliation, chemical exfoliation, chemical synthesis, and thermal chemical vapour deposition (CVD). Mechanical exfoliation is the first observed method of graphene synthesis (Bhuyan *et al*., 2016). Graphene sheets which are produced using this method showed high quality, in comparison with other methods, with lateral sizes up to 100 µm (Booth *et al*., 2008).

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Graphite is a naturally occurring mineral containing millions of single layers of graphene flakes stacked by weak Van der Waals forces, to form the rocks (Bhuyan *et al*., 2016). Graphite forms when carbon experiences heat and pressure from the Earth's crust and upper mantle. Even though several countries all over the world mine graphite, Sri Lankan graphite is known as the best graphite, with some of the deposits having carbon content up to 100% (Dissanayake, 1981; Handl, 2021). Unlike the other graphite deposits in the world, the graphite deposits in Sri Lanka are formed as a result of cooling and reduction of atmospheric CO_2 (Touret *et al*., 2019; Handl, 2021). Kahatagaha, Kolongaha, and Bogala are the main graphite mines found in Sri Lanka. Graphite occur in various morphologies, with different physical and structural characteristics like plate, flake, and fibrous graphite (Wevitavidana *et al*., 2012). However, Sri Lanka is still exporting bulk graphite as a raw material. Recently, Sri Lankan scientists started working on value addition to graphite and exploring the potential applications of Sri Lankan graphite. Somaweera *et al*. (2021) reported the mechanical and thermal properties of Sri Lankan vein graphite powder. Manoratne *et al*. (2017), have studied the structural and optical properties of graphene oxide fabricated from high purity Sri Lankan vein graphite. The Sri Lankan graphite can be used for solar energy generation and storage (Gao *et al*., 2017; Manoratne *et al*., 2017; Amaraweera *et al*., 2018; Gunasekara, 2021) and water purification applications. Jayamaha *et al*. (2017), demonstrated an electrochemical double layer capacitor made with PEO and Sri Lankan natural graphite. However, there were no attempts made to study the electrical characteristics of Sri Lankan graphite.

In this work, the methods to make graphene FETs were explored, using commercial grade Sri Lankan graphite obtained from Kahatagaha mines with a purity of 97% as the graphene source. A single layer of graphene sheets was successfully separated, followed by transferring the substrate and demonstrating the application for FETs. The electronic properties including electron and hole mobility were also studied.

MATERIALS AND METHODS

Large chunks of commercial grade graphite (purity 97%) from Kahatagaha mines, Sri Lanka, were used for our study. A piece of graphite was selected with highly oriented graphite layers as shown in Figure 1(a). From the large piece, a small piece of graphite was selected carefully to obtain exfoliated graphene with larger area. The selected piece of graphite is shiny and smooth, which is an indication of the presence of large pieces of graphene flakes as illustrated in Figure 1(a). Then graphene was exfoliated from the selected piece of graphite using the Scotch tape method, as described in Figure 1.

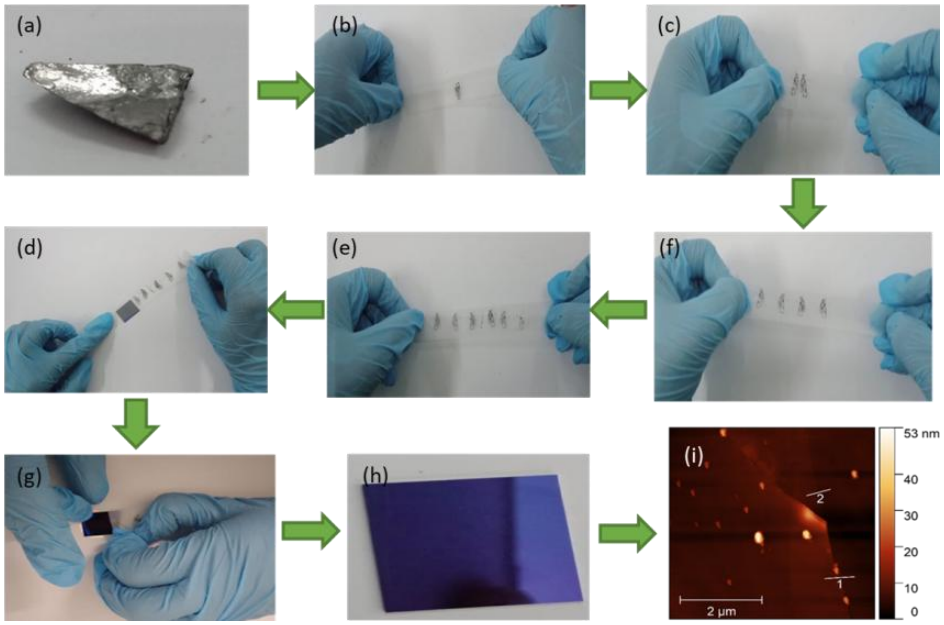

Figure 1: Photographs showing (a) selected piece of graphite for graphene extraction; (b) to (f) successive scotch tape peeling method of graphene layer and (g) graphene transferred on to SiO_2/Si substrate; (h) graphene transferred SiO_2/Si substrate and (i) AFM image of the transferred graphene layer

As shown in the Figure 1(b) to 1(f), graphene was repeatedly peeled off several times using Scotch tape. This procedure was repeated until all possible single graphene layers were obtained. Subsequently the graphene layer was transferred to the silicon wafer chip as shown in Figure 1(g). After that, the important features of the graphene layers were examined using an optical microscope and atomic force microscopy (AFM). The AFM images were used to measure the thickness of graphene layers. Back-gated graphene FETs were fabricated using mechanically exfoliated monolayer graphene. Fabrication of graphene FET using the silicon substrate as a back gate is an enchanting method. In this study, Scotch tape was used to peel off graphene layers from large graphite chunks.

The graphene FET was fabricated by depositing source and drain electrodes on the graphene sheet using thermal evaporation under vacuum (Thanihaichelvan *et al*., 2018, 2019; Murugathas *et al*., 2019). A shadow mask with a channel length of 5 µm and width of 1 mm was used to define the source and drain electrodes. The effective channel width was measured by using an optical microscope. These graphene FETs were then electrically characterized by using a computer interfaced source measuring unit (Keithley 4200) at room temperature (Thanihaichelvan *et al*., 2022). The circuit connections used for measurements, along with the schematic of the fabricated FET, are illustrated in Figure 2. The transfer curves of the fabricated FETs were measured by sweeping the gate voltage from -40 V to 40 V with a supply voltage of 10 mV.

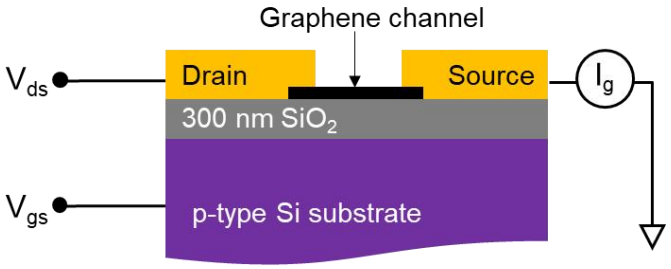

Figure 2: Schematic diagram of graphene FET with circuit connections to study the electronic properties of the FET

RESULTS AND DISCUSSION

The graphene-transferred SiO_2/Si substrate was examined under an optical microscope, and the image captured using a charge-coupled device (CCD) camera is shown in Figure 3(c). The bright yellow area in the middle represents multiple layers of graphene. Layers of graphene in circled areas marked X and Y were tested with AFM for thickness calculations.

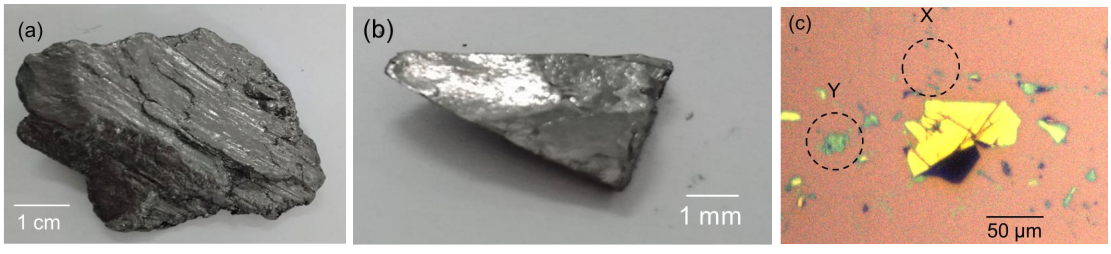

Figure 3: Photograph of (a) a large piece of graphite received from Kahatagaha mine; (b) a selected small piece of graphite for graphene exfoliation, and (c) the optical microscope image of the transferred graphene sheets on the SiO_2/Si substrate.

Structural properties of graphene layers

AFM images were used to measure the thickness of the deposited graphene layers. The thickness of graphene sheets arranged between the source and the drain contacts were identified by line scanning across the possible graphene-substrate interface from the AFM images taken on the graphene sheets. The AFM images and their line profiles are depicted in Figure 4, and the thickness of the graphene layers in the channel was determined. As in Figure 4(a) two different contrasts can be seen and this indicates the presence of two different layers one stacked on another. Three-line profiling across both surfaces was done, and is shown in Figure 4(b). From Figure 4(b) it was possible to determine, across the line 1, that the thickness is about 0.9 nm and across the line 2, the thickness is about 0.4 nm. Theoretically, the thickness of a single layer graphene is about 0.335 nm. So, it can be confirmed that the thickness across the line 2 is approximately equal to the thickness of monolayer graphene and the line profiling across line 1 corresponds to two layers of graphene.

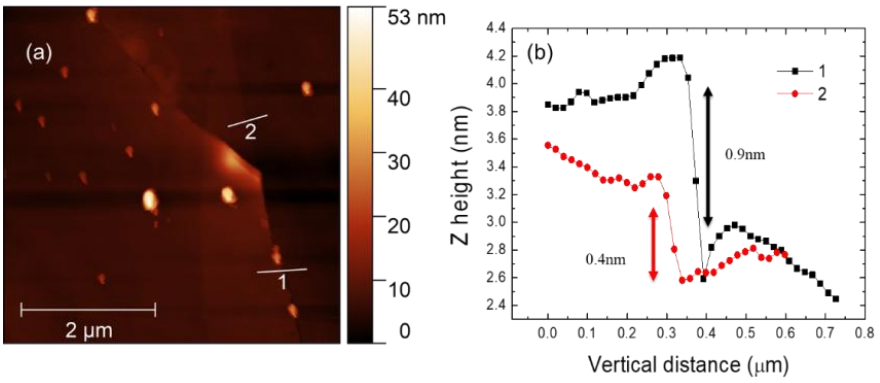

Figure 4: (a) AFM image with two different layers of graphene transferred onto the SiO_2/Si substrate; (b) line scanning data taken across lines named 1 and 2 in the AFM image.

Again, the AFM images were taken on the transferred graphene marked in circle Y as indicated in Figure 3(c), and are shown in Figure 5(a). Figure 5(a) shows the graphene-substrate interface. After the AFM test the line profiling was done and all three lines confirm that the thickness of graphene layer is about 0.4 nm, which is consistent with the thickness of monolayer graphene. The AFM studies on the transferred layer confirmed the presence of single layer graphene on the substrate.

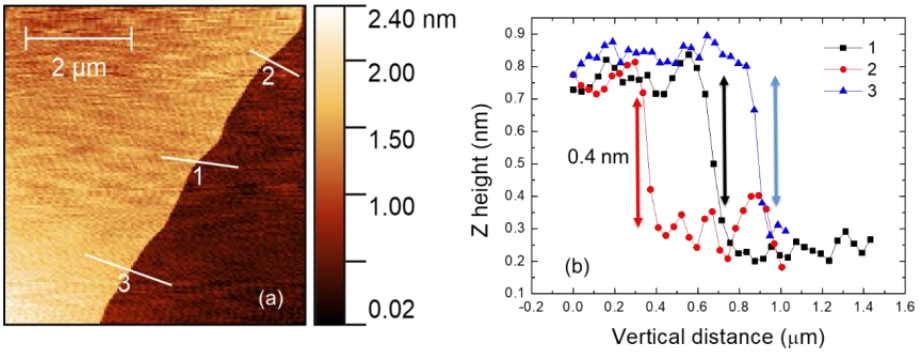

Figure 5: (a) AFM image with a monolayer of graphene; (b) the line scanning profile for the monolayer of graphene across the lines named 1, 2, and 3 in the AFM image.

Electronic properties of graphene FET

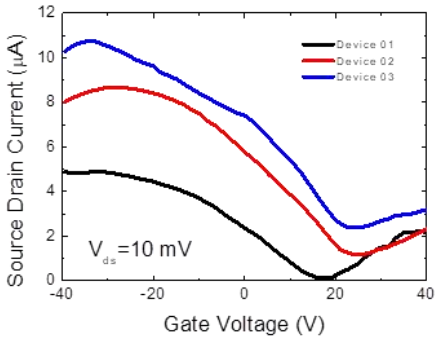

Figure 6: Transfer characteristic curves of three graphene FETs made from graphene

Transfer characteristics can be determined by observing the source-drain current with variation of gate-source voltage. The FET were made by depositing the source and drain electrodes using thermal evaporation. A total of 24 devices were fabricated and 3 of them showed field dependent conductance. Figure 6 shows the transfer characteristic graph of three of the tested graphene FET devices and the electrical properties of all three graphene FETs were summarized in Table 1.

Table 1: Electronic parameters of tested graphene FETs

	On-current (μA)	On-off ratio	Dirac voltage (V)
Device 01	4.8	44	17
Device 02	8.0	7.5	24
Device 03	10.2	4.53	22

The transfer curves show ambipolar behaviour with an on-current of 4.8 to 10.2 μA for a relatively lower source-drain voltage of 10 mV. It is well known that graphene is an ambipolar material and the graphene FET can have a minimum conductance (Dirac point), with varying gate voltage. Theoretically, the Dirac point of an intrinsic graphene FET must be zero volts as the band gap of graphene is zero (Geim & Novoselov, 2007; Reddy *et al*., 2011). However, the Dirac voltage of a graphene FET can be shifted positively or negatively due to the dopants and charged molecules on the graphene surface (Ohno *et al*., 2015; Andronescu & Schuhmann, 2017; Lee *et al*., 2018). As shown in Figure 6 and Table 1, for all three fabricated FETs, the Dirac voltage is found to be positive (+17.0, +22.0 and +24.0 respectively), which indicates that the graphene layer is p-type doped (Murugathas *et al*., 2020). This positive Dirac point shows the hole dominated conductance of the fabricated graphene flakes at zero gate voltages. This can be attributes to the presence of oxygen species in the graphene surface (Ohno *et al*., 2015). Sri Lankan graphene also contains sulphur as a common impurity, which can also produce a positive Dirac voltage (Murugathas *et al*., 2020). The on-off ratio of the fabricated FETs was found to be 44, 7.5 and 4.53. The relatively lower on-off ratio is also a common observation for graphene FETs with channel widths of more than 1 μm (Yang & Murali, 2010; Reddy *et al*., 2011; Crosser *et al*., 2015). A high on-off ratio of 44 was observed for device 1. This could be due to the narrow channel width and edge effects during the charge transport.

The mobility of the carriers is an important variable to understand the performance of graphene-based devices. The direct transconductance method was used to calculate the mobility of fabricated FETs. The transconductance (g_m) value was calculated from transfer characteristics.

The field effect hole and electron mobility values were calculated using the following equation:

$$\mu = \frac{g_m L}{WCV_{ds}}$$

where L is length of the channel, W is width of the channel, and C is the specific capacitance of gate oxide (300 nm thickness of SiO_2). The transconductance $g_m = \left(\frac{\partial I_{ds}}{\partial V_{gs}}\right)$ was calculated from the linear region of the transfer curves. The electron mobility was found from the right side of the curve and the hole mobility from the left side of the curve. The calculated mobility values are given in Table 2 for all three tested FET devices.

Table 02: Electron and hole mobility values of fabricated graphene FETs

	Electron mobility ($cm^2V^{-1}s^{-1}$)	Hole mobility ($cm^2V^{-1}s^{-1}$)
Device 01	282.2	592.2
Device 02	287.1	717.5
Device 03	186.0	465.8

The mobility values found in this work appears to be low, which could be due to the scattering contribution from the SiO_2 substrate or the graphene layer. It was also noted that commercial grade graphite with a purity of 97% was used for FET fabrication. It was also noted that the hole mobility was relatively higher than the electron mobility in all three tested devices. This indicates that the electrons in the Sri Lankan graphene have relatively higher effective mass when compared to the holes. The mobility asymmetry and higher hole mobility has also been observed and reported in many other graphene FET studies (Lu *et al*., 2012; Liang *et al*., 2015; Urban *et al*., 2020).

CONCLUSION

In summary, graphene sheets were successfully exfoliated from Sri Lankan graphite using the Scotch tape method and graphene FETs with a global back gate geometry were fabricated. AFM images were used to confirm the existence of single layer graphene in the substrate. It was found that the fabricated graphene FETs showed an ambipolar current response with a positive Dirac voltage. The mobility values varied from device to device, and it was noted that the electron mobility of the FETs was smaller than the hole mobility, indicating the increased effective mass of electrons in Sri Lankan graphene.

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