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RESEARCH COMMUNICATION

Implementation of data cache block (DCB) in shared processor using field-programmable gate array (FPGA)

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Abstract: This research deals with a novel dynamic reconfigurable multiprocessor technique combined with a System-On-Chip (SOC) and provides continuous transition activities in a digital environment. It also provides transition noise in the frequency domain than time domain. The reconfigurable model achieves optimal output in terms of area and latency. A two-tier implementation which is based on chip clock scheduling is proposed. To develop and eliminate crystal noise, this research develops two different logics i.e., consumption of current and settling time. Here, Data Cache Block (DCB) is used to control all other operations. The proposed work is used to minimize power consumption through an inverter amplifier and a shared processor is used to reduce the system cost and increase performance.

Keywords: Dynamic reconfiguration, MPSoC, multiprocessor.

INTRODUCTION

Hardware accelerator

In multiprocessor architecture (Saurabh & Shah, 2016), hardware accelerators are used to implement the application-specific instructions. Use of application-specific instructions is the best way to develop multiprocessor performance. In multiprocessors (Fan *et al*., 2016), hardware accelerators are used to reduce implementation time. The mixed integer program (MIP) is used to minimize the execution time under a required limit for space exploration. To achieve the required performance and area coverage, MIP model is used to analyse multiprocessor configuration. This architecture is better than conventional architecture in terms of system cost, energy and performance (Zhang *et al*., 2016).

In improving the performance of a hardware accelerator system, a shared processor plays a vital role in cost reduction. It contains different configurations as shown in Figure 1. The design space exploration (DSE) (Ananda Krishna & Yadav, 2016) improves the performance of the heterogeneous multiprocessor configuration and also reduces the usage of field-programmable gate array (FPGA) resources with reduction in area usage (Alderson *et al*., 2016).

Multi accelerator

A multi-accelerator combined with a reconfigurable block and partly reconfigurable architecture was used for various applications by means of executing multiple regions (Figure 2). The multiple regions of the multi-accelerator are reconfigured at independent intervals. The designed architecture consists of a processor, controllers and partially reconfigurable multiple regions.

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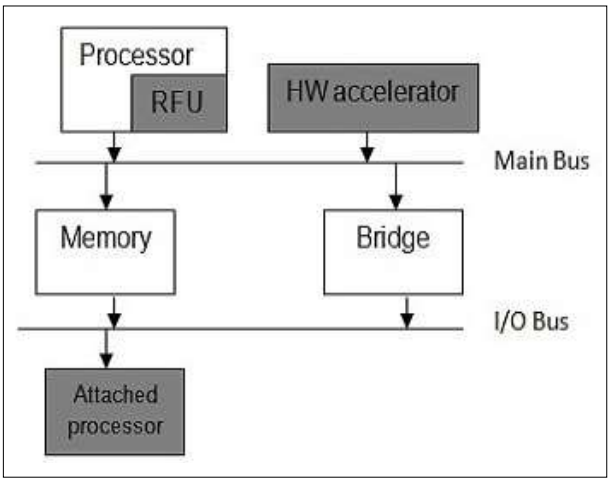

Figure 1: Coupling schemes of dedicated hardware components

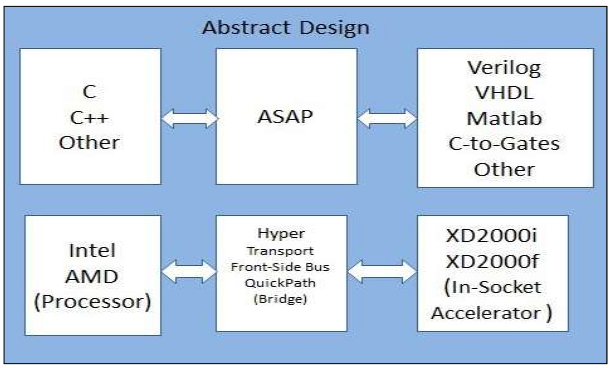

Figure 2: A systematic block for hardware accelerator

The reconfigurable form is made with a different type of architecture. To analyse the different heterogeneous multiprocessors, hardware accelerators are arranged in systematic order (Karthick *et al*., 2017a; b). But in anti-symmetric form, all processors are different from each other (Karthick *et al*., 2017c). In conventional method, the FPGA circuit includes minimum amount of resources whereas some analytical methods are calculated from the simulations experiment (Karthick *et al*., 2018).

Cache in processor

Each center of a multi-core processor features a devoted L1 store and is mostly not divided among the centers. The L2 store, and more elevated level reserves, can be divided among the centers. L4 reserve is at present unprecedented and is for the foremost part on (a type of) dynamic random-access memory (DRAM) rather than on static random-access memory (SRAM), on a special bite the dust or chip (outstandingly, the structure, DRAM is employed for all degrees of cache, right down to L1). DRAM is utilised for all degrees of the cache, right directly down to L1. That was the case generally with L1, while greater chips have permitted the incorporation of it and regularly all store levels, with the conceivable special case of the last level. Every additional degree of cache will in general be greater and enhanced in an unexpected way.

The data cache block in the shared multi-processor achieves better performance in relation to area, latency and power consumption. Figure 3 shows the shared cache in processor.

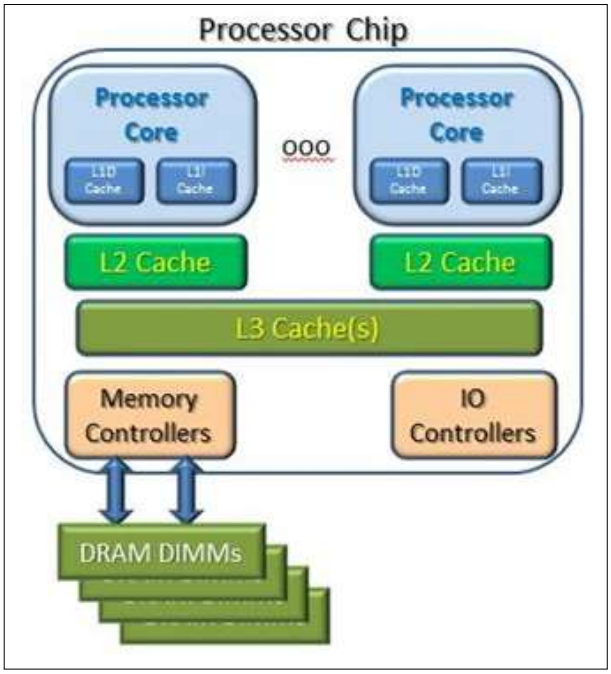

Figure 3: Shared cache in processor

Dynamic optical reconfigurable logic block

A logic block with optical reconfiguration has a multiplexer, flip flops and buffers with preset functions. The switching activities play a major role in transferring Look up Tables (LUTs) via different channels with reconfiguration blocks. The LUTs are used by means of Demorgan's theorem. The delay flip flops are mixed with multiplexer (MUX) for LUT configurations.

Most of the multiplexes are used in combinational as well as sequential circuits. The reconfiguration block contains photodiodes with LUTs and photodiodes with tri-state buffers. To develop dynamic reconfigurations by using recent very-large-scale integration (VLSI) chips, fast arrangements of outputs are not at all impossible.

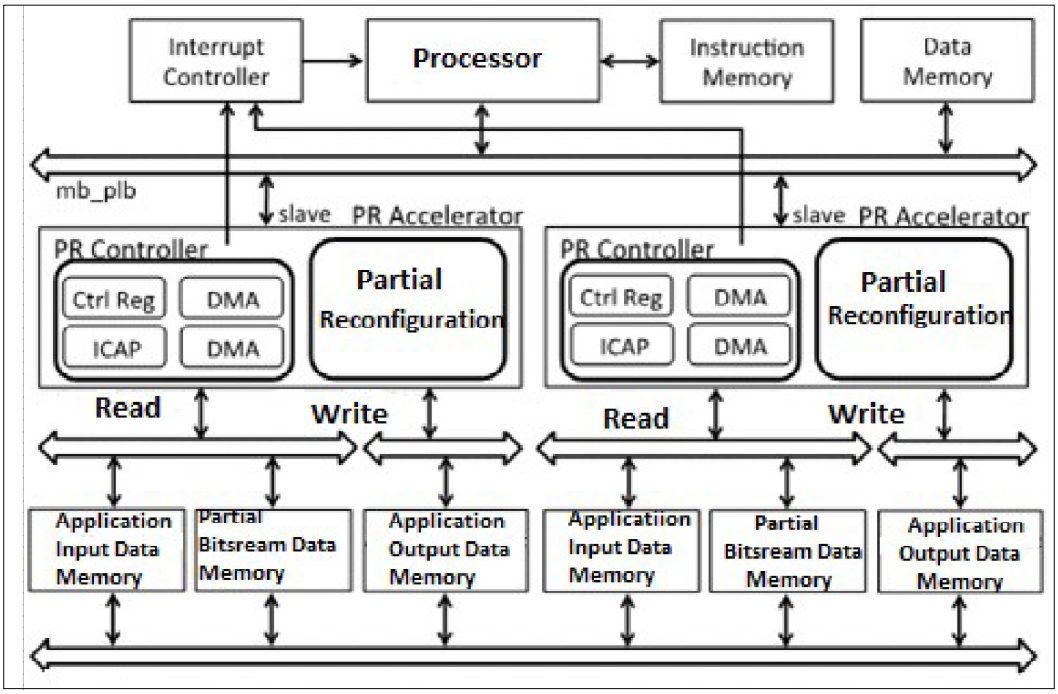

Figure 4: Proposed dynamic reconfigurable processor architecture with a multi-accelerator

Today, the tri-state buffers with mux connected to proper channels are available. The other techniques are implemented by optically dynamic reconfigurations.

METHODOLOGY

A novel partial reconfigurable processor architecture

A partial reconfigurable (PR) controller and a multi-bus system are two important features in the proposed architecture. The partial reconfigurable controller is used for all blocks in architecture such as the accelerator and execution unit. To transfer data, minimization of delay bus is required. Figure 4 shows the block diagram of proposed architecture.

A PR region and PR controller combines to generate a PR accelerator that consists of six buses with instruction memory, micro blaze processor, data memory, and slave ports. Processor Local Bus (PLB) is another important bus unit in PR reconfigurable block. The memory application data is combined to the bus with the port of partial reconfigurable controller (write master).

Table 1: Performance comparison of area, speed, power and latency

Performance Metrics	Area	Speed	Power Consumption	Latency	Error
Device: Virtex 6 Family XC6VLX75ti Package: ff484 Device Power: 435 m watts					
EXISTING SYSTEM	350 Slices	226.16MHz	78.2%	4.422ns	60
PROPOSED SYSTEM	296 Slices	340.53MHz	72.6%	2.937ns	59

There is a dual-port memory controller used to generate input and output data with partial reconfiguration. A host PC accesses the controllers with mb_plb, which is connected to a processor.

RESULTS AND DISCUSSION

The experimental results give comparison of power consumption, area, speed and latency for dynamically reconfigurable processor with FPGA circuit. Table 1 shows performance comparison for area, speed, power consumption and latency.

Figures 5(a), (b), (c), (d) show a comparison of performance measures of the proposed system and the existing system. The results have been taken from Xlinix software with the FPGA platform. Figure 5(a) shows the area in terms of slides; here, a comparison is made between the existing and proposed system. The slides are reduced to 295 from 350. As per Figure 5(b), the processing speed will be improved from 225MHz to 340 MHz. The power consumption [Figure 5 (c)] also will be reduced, in proposed system (72.5 percent). Lastly, the latency [Figure 5(d)] of the proposed system is low when compared to the existing system.

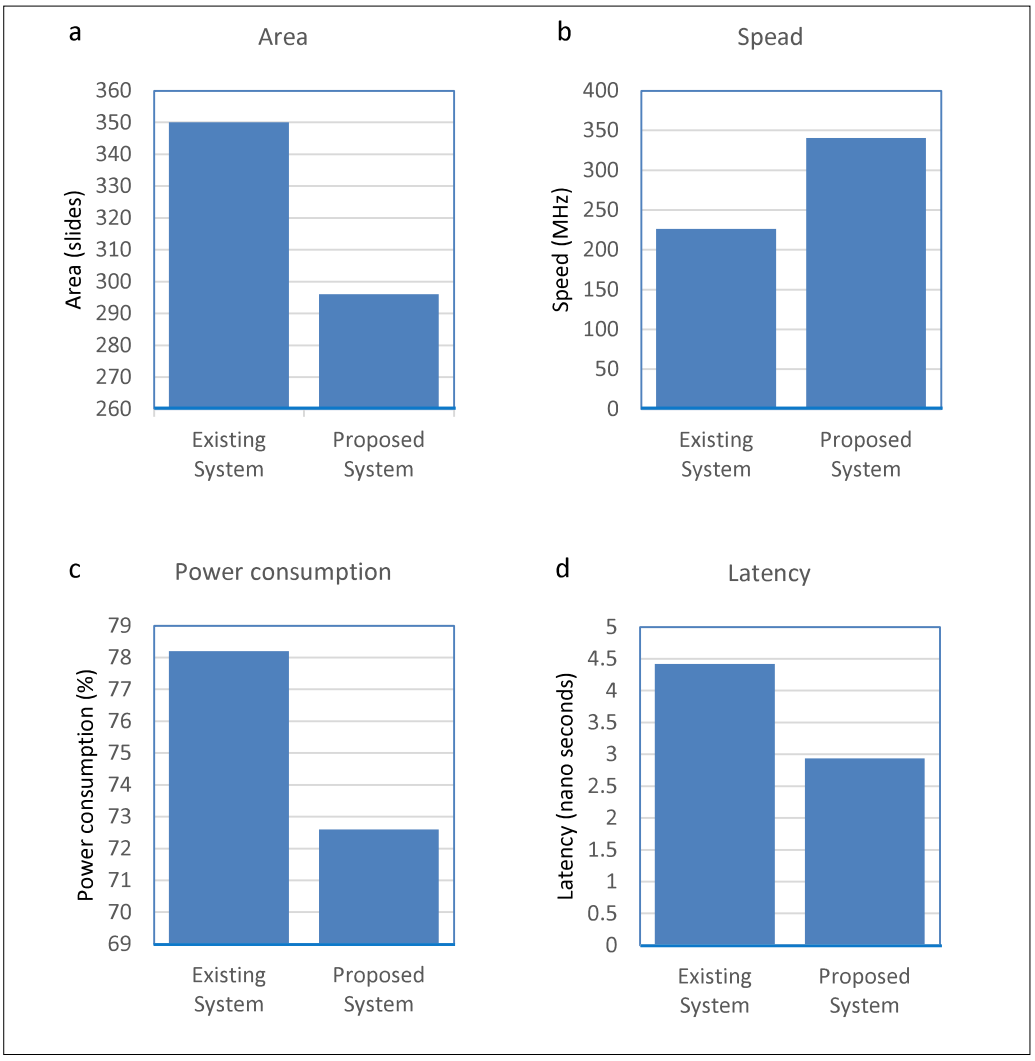

Figure 5(c): Comparison of power consumption on base work vs proposed work.

CONCLUSION

The proposed architecture contains a novel multiprocessor with hardware accelerators combined with several processors used to minimize overall system cost and improved performance. The experimental values make better performance with fewer reconfigurable blocks rather than multiprocessor architecture. Here, reconfiguration methods are presented to design space of multiprocessor with reasonable time frame. In multiprocessor architectures, the various application patterns have been implemented for shared hardware with FPGA environment. Experimental results show that the proposed dynamically reconfigurable multiprocessor system has reduce the power consumption from14.2% to 14% and area/latency trade-off is calculated rapidly.

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