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RESEARCH ARTICLE

Constant frequency control of an Active Power Filter

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Abstract: Active Power Filters (APFs) improve the electricity supply by correcting harmonic distortions created by non-linear loads. It also corrects the poor power-factor resulting from inductive loads. Topologies and control techniques available for APFs are numerous. This paper considers a single phase APF. A scheme that requires minimum calculation burden has been selected. The system considered, uses an unified constant frequency integration control that gives a minimum calculation burden and faster response. The control method adapted requires sensing the load current and DC-link voltage only. However, it causes some problems at the integration level. The analog integrator gives some initial voltage when operated at high frequencies due to inability to reset the integrator fully. To avoid errors due to offset in the integrator, an offset feedback is proposed and tested in this study. The control is simulated and the results are validated with laboratory experimental waveforms.

Key words: Active power filter, harmonic elimination, harmonic filter, passive filter, PQ-theory, reactive power compensation.

INTRODUCTION

Power electronic loads form a major issue on the quality of power of any electricity supply that feeds such loads. The harmonic currents injected by the loads into the power network, distort the network voltage. Propagation of harmonics may lead to a severe voltage distortion, when the network is weak. Non-linear loads add much to the problem. Lower efficiency, harmful interference to neighbourhood appliances, overheating the transformers and malfunction of the sensitive equipment could be the result. Therefore, a reduction in the power quality[1,2] is inevitable. In addition, the harmonic-current would increase the rating of the capacitor banks used for power factor correction.

The reactive current in the network causes poor power-factor operation. This is due to inductive loads such as induction motors, arc welders, inductive ballast florescent lamps and power transformers. The poor power factor increases the loss in the transmission network and also reduces the network voltage.

Currently the government is studying several energy saving proposals to reduce the losses and increase the electrical connections to the public. Projects on improving the power-factor and eliminating-harmonics are therefore of vital importance as given in the government proposal.[3]

1.1 Power factor improvement and harmonics elimination methods:

Capacitor banks are typical in power factor correction for inductive loads. However, most of the industries are equipped with harmonic loads such as adjustable speed drives and automated computer control equipments to increase their energy efficiency.[4-8] The harmonic loads introduce an additional requirement of harmonic filters, when power factor correction is made using banks of capacitors.

Also the passive harmonic-filters and power-factor correction capacitors possess a disadvantage when harmonic loads present in the neighbourhood of the electrical network are on a Point of Common Coupling (PCC). Loads on a PCC can increase the rating of elements forming the passive-filters and capacitor banks that are on the same PCC. The reason is that the harmonics created by other customers may also get into a filter network of a different customer, overloading the filters, which are not designed for unexpected loads.

Developments in semiconductors and their packaging technology have enabled power electronics at high frequency applications.[9] Therefore, to solve problems in power systems, power electronics can play a bigger role. The emergence of these new devices has led to researchers around the world to propose several Active Power Filter (APF) control techniques.[10-12]

Mainly two APF configurations are being studied; (i) shunt APF and (ii) series APF with shunt passive filters. The shunt APF directly controlls the current. Therefore, this configuration is most suitable to this APF

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current sources, in which the harmonic loads have high internal impedance for harmonics compared to the grid impedance. The series APF act as high impedance for harmonics while maintaining low impedance at fundamental frequency. Therefore, the series APF pushes the harmonic current in to the shunt passive filter and prevents harmonic current flowing into the grid system from the specific harmonic loads. This configuration is most suitable to compensate harmonics produced by the harmonic voltage sources, in which the harmonic loads have low internal impedance for harmonics compared to the grid impedance.

Many control techniques have been studied. In these techniques, several methods are used to extract the control signal, which determines the injected voltage and/or current from the APF. The control signals are extracted using (i) instantaneous active and reactive power theory, (ii) Space vector techniques, (iii) Phase lock loop techniques and (iv) Fast Fourier Transformation techniques. Different inverter controls are used to produce Pulse Width Modulation (PWM) signal from the control signal. Mainly used PWM techniques are Sine-triangular, Hysterisis, Selective harmonic elimination, Regular sample and Space vector.

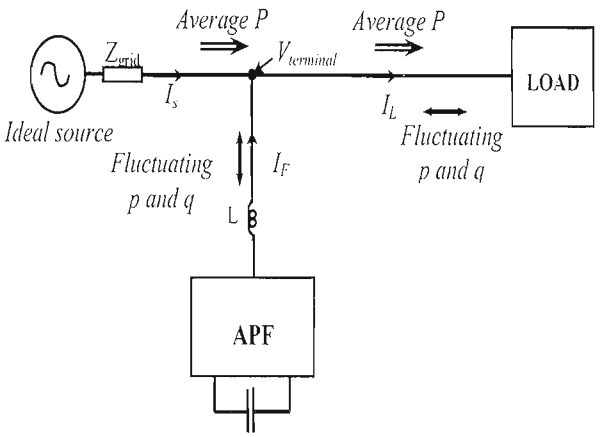

Figure 1: Block diagram of the proposed Active Power Filter (APF)

2 PROPOSED ACTIVE POWER FILTER

2.1 Principle of constant frequency integration control

Figure 1 shows a shunt connected APF.[12] The APF injects exact amount of current, I_F, which is required to cancel the harmonic and reactive current components generated by the load. Therefore, the current drawn from the source will be purely sinusoidal and in-phase with the supply voltage.

2.2 APF control circuit

Figure 2 shows the schematic diagram of the control circuit. As seen, the control method has two decoupled loops, the current control loop, and the DC voltage control loop.

Current control loop : The error is estimated from the source current measurement. When a harmonic load is introduced, harmonic content introduces a disturbance as an error in the source current. The control circuit finds the switching instants so that the duty ratio required to compensate the error is achieved. Thus it does make faster compensation, since the duty required for instantaneous current requirement is implemented within the sample period.

Voltage control loop: The error is estimated from the DC-link voltage measurement (DC-link control loop) The DC-link control loop maintains the capacitor voltage at a set reference value using feedback action. The error at the DC-link is regulated by a PI controller, and the PI controller output Vm is added to the current control loop to vary the duty ratio to maintain the DC-link voltage.

2.2.1 DC-link voltage of the APF

The DC-Link voltage can be calculated using the volt-second balance of the inductor, in steady-state, as shown below.

Let,

fs : Switching frequency
Ts : Switching period
D : Duty ratio of the switch A (ON-state-period / Total-period)
Vs : Source voltage
Vc : DC-link voltage
V_L : Voltage across Inductor L

Then,
For $0 \le t \le D \cdot Ts$ *A-ON & B- OFF*
Applying Kirchoff 's Voltage,
$V_L = V_S + V_C$
For $D \cdot Ts \le t \le Ts$ *(A-OFF, B-ON)*

volt-second balance across the inductor in steady state gives,

$$(V_C + V_S) \cdot D \cdot T_S = (V_C - V_S) \cdot (1 - D) \cdot T_S \quad (1)$$

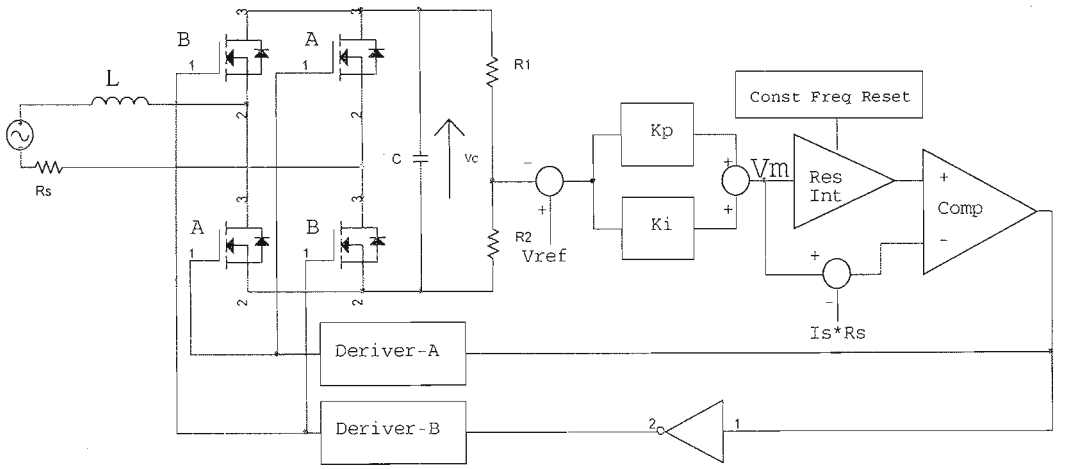

Figure 2: Schematic diagram of the control circuit

Equation (1), yields:

$$= \frac{V_S}{(1-2D)} \tag{2}$$

2.2.2 Functions of the control circuitry

a) Equivalent resistance seen by the source in the power circuit

Figure 3 shows equivalent circuit diagram of the system. The total load impedance across the source terminal is indicated by R_e. The R_e becomes a pure resistive component when the APF is compensating the harmonic and reactive current of the non-linear load. Therefore, when the APF is in operation, the net current drawn from the source becomes same as the fundamental active power current component absorbed by the load.

$$V_S = I_S \cdot R_e \tag{3}$$

Where R_e is the effective resistance seen by the source.

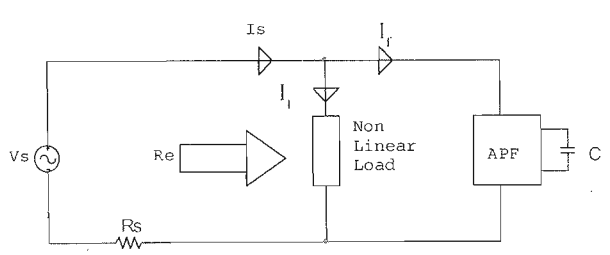

Figure 3: Equivalent circuit diagram of the system.

b) Calculation of the duty ratio D

From equations (2) and (3)

$$\frac{R_S}{R_e} \cdot (1-2D) \cdot V_C = I_S \cdot R_S \tag{4}$$

By assuming,

$$V_m = \frac{R_S}{R_e} \cdot V_C \tag{5}$$

This becomes,

$$2D \cdot V_m = V_m - I_S \cdot R_S \tag{6}$$

Taking V_{INT} as the output of the resettable integrator,

$$V_{INT} = \frac{1}{T} \cdot \int_0^{DT_S} V_m \cdot dt \tag{7}$$

Assume that within the switching period T_S, V_m remains constant (see equation 5).

V_{INT} can be written as,

$$V_{INT} = \frac{1}{T} \cdot V_m \cdot D \cdot T_S \tag{8}$$

The integral constant is selected in such a way that satisfied equation (6). Then the integrator time constant

compensate harmonics produced by the harmonic (T) becomes $T = {}^{Ts}/_{2}$, thus equation (8) can be written as:

$$V_{INT} = 2D \cdot V_m \tag{9}$$

In the comparator circuit

Input at the positive terminal of the comparator $(V+)$ is

$$V+ = V_{INT} = 2D \cdot V_m$$

Input at the negative terminal of the comparator $(V-)$ is

$$V- = V_m - I_s \cdot R_s$$

As the inputs $(V+)$ and $(V-)$ are compared with no hysteresis, the comparator output gives high and low time durations, which are used to switch the inverter switches, in order to satisfy equation (6).

Equation (2) is always valid, and equation (6) is derived by the control circuit. Therefore equation (3) becomes valid; hence the source delivers current to the system, which is equivalent to a resistive load (R_e). This shows that the APF maintains the supply current sinusoidal and in-phase with the supply voltage.

2.3 Resettable integrator

The gate pulses of the switches were obtained by comparing a voltage ramp with a constant voltage produced by the controller. A resettable integrator was used to produce the ramp. However, the resetting of the integrator was not perfect.

2.3.1 Problem of the resettable integrator

Figure 4 shows the output of the resettable integrator. A capacitor is used at the output of the conventional Op-Amp integrator and a switch operated at switching frequency to discharge capacitor. Since the switch has a small on-time voltage and internal resistance, the capacitor cannot be discharged to zero voltage. Finally this operation leads to an offset voltage, V_{off}, across the capacitor. Therefore this non-ideal characteristic of the switch introduces an offset voltage at the integrator output.

Assume that the integrator-offset voltage is V_{off}, then,

$$V_{INT} = 2D \cdot Vm + V_{off} \tag{10}$$

substituting from (10) in (6) for new V_{INT}:

$$2D \cdot Vm + V_{off} = Vm - I_S \cdot R_S \tag{11}$$

From equations (2), (5) and (11), the supply current can be written as

$$Is = \frac{V_S}{R_e} - \frac{V_{off}}{R_S} \tag{12}$$

Since the sensing resistance is small, the offset in the supply current will be significant even for a small offset voltage. This offset shifts the zero crossing point and causes malfunction to the controller. Also this orthogonal DC-offset line current introduces an additional unwanted resistive loss in the circuit.

2.3.2 Solution to the resettable integrator offset voltage

Figure 5 shows an auxiliary integrator circuit, which eliminates the offset at the output of the resettable integrator. Here the auxiliary integral controller regulates the offset current to get a negative voltage. Then this output is added to the resettable integrator output to cancel the offset effect.

3 EMTDC/PSCAD SIMULATION OF ACTIVE POWER FILTER CONTROL TECHNIQUE

The proposed APF control was simulated using PSCAD Version 4.0. Current waveforms of the APF, Load, and the Source were plotted when the source rms voltage Vs = 100 V, and the frequency f = 50 Hz. The DC-link voltage was set to 200 V. The switching frequency of the power MOSFET is set by resetting integrator at a constant frequency of 50 kHz.

Figure 6 shows the schematic PSCAD simulation diagram of the APF. In this circuit, a pre-charging arrangement is added to the DC-link capacitor to charge the capacitor during the startup period. The charging arrangement is disconnected using a circuit breaker after a specified time. An auxiliary loop has been added to

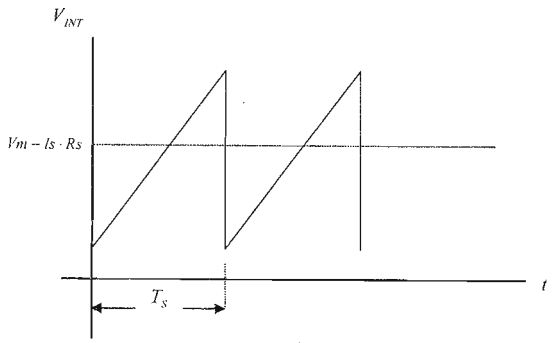

Figure 4: Integrator output with offset voltage

control technique to eliminate the DC-offset voltage caused by the resettable integrator. In the auxiliary loop, a PI controller is used to regulate the error and eliminate the DC-offset voltage. The simulation was carried out for several types of harmonic and poor power factor loads. Results show excellent performance of the proposed APF, which compensates for the harmonic and reactive power currents independent of the load types.

4 LABORATORY SETUP OF THE ACTIVE POWER FILTER

4.1 Circuit diagram of the control circuitry

Figure 7 shows the control circuitry used to implement the proposed APF. High frequency (high slew rate) op-amp LM 318 is used for the resettable integrator and a DG411 analog switch is used to reset the capacitor of the resettable integrator. The values of resistances, used in the resettable integrator, are selected with 100 kΩ to reduce the loading effect at the voltage *Vm* and all other fixed resistances have the value of 10 KΩ. LM 324 op-amp is used for all the other application circuits.

4.2 Driver circuit and protection for the DC-link

Figure 8 shows protection and driver circuits. Here two IR 2104 ICs are used to drive the power MOSFETs of the single-phase H-bridge. The IR 2104 driver has a shut down terminal (SD), which gives off signal to all the MOSFETs when the SD terminal voltage becomes less than 2.5 V. This facility is used for the fast protection to the DC-link voltage.

RESULTS

EMTDC/PSCAD simulation results obtained with non-linear load.

Figure 9 shows the simulation results of source voltage and current waveforms when a full- bridge diode rectifier load is connected. The results show that the load produces heavy harmonic current. The APF injected current and source current waveforms show the excellent compensation of the proposed device even for a higher harmonic load. The second graph shows that the APF maintains the source current not only sinusoidal but also in-phase with the source voltage with this load.

Laboratory experimental result obtained for the bridge rectifier load

Figure 10 shows the experimental results of source current waveforms with the bridge rectifier load. Figure 10 (a) and (b) were taken respectively without and with the APF. This shows clearly that with the APF, the source current is free from the heavy harmonic current produced by the load. Also the similarity of Figures 9 and 10 shows a strong validation of the simulation and the experimental results.

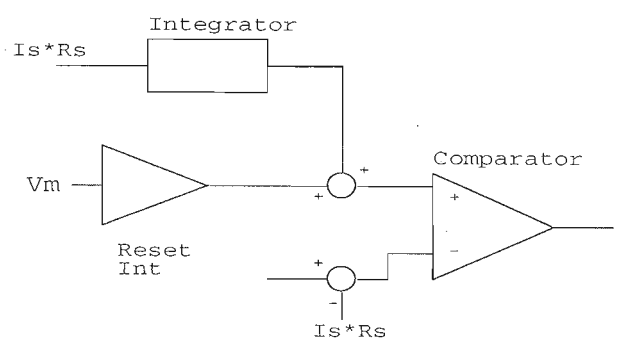

Figure 5: Elimination of offset voltage by an integrator loop

CONCLUSION

An APF control is proposed with detailed mathematical derivation considering offset at the analog integrator. This control is simulated using EMTDC/PSCAD computer package. Finally a laboratory model was designed and the proposed APF was tested successfully. The simulation and experimental results validate the proposed control technique.

There are four major advantages with this APF: (i) The control algorithm is implemented by a simple cost effective hardware instead of a costly DSP system. Therefore it is suitable for small industries, (ii) The rating of APF depends only on the particular load and neighbourhood loads do not affect it, (iii) This APF is not only used to eliminate harmonic currents but also used for power factor correction, (iv) The APF guaranteed that no offset would be in the source current.

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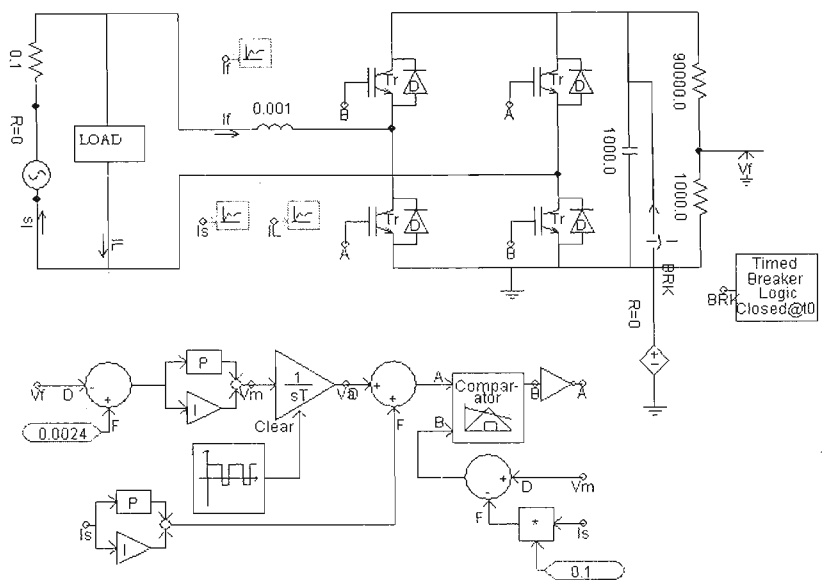


Figure 6: PSCAD Simulation schematic diagram of APF

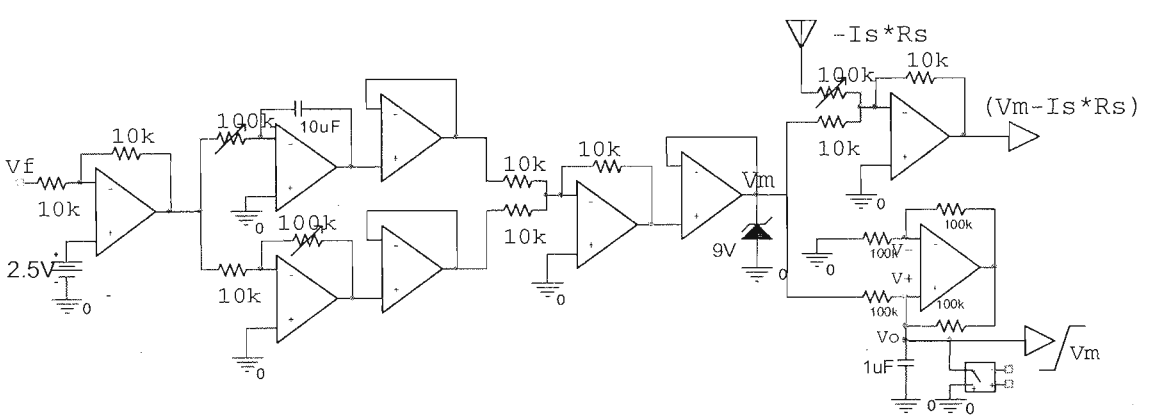


Figure 7: Simplified hardware control circuitry

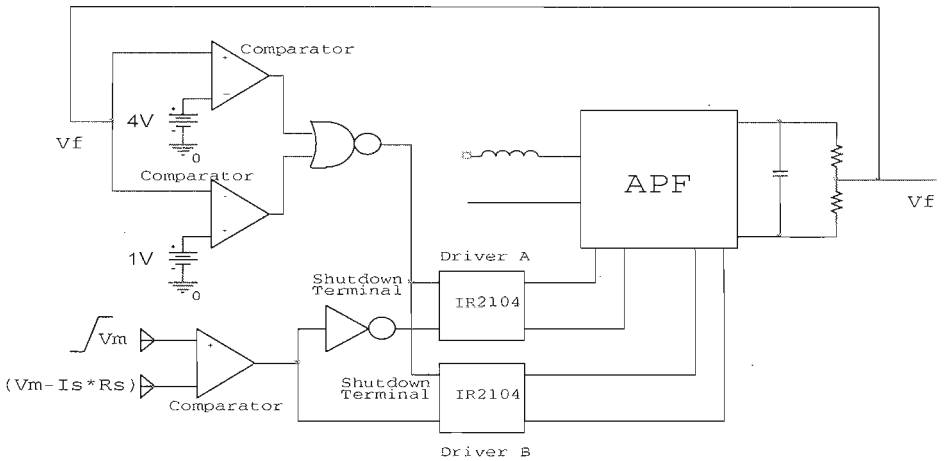


Figure 8: Simplified hardware protection and driver circuitry

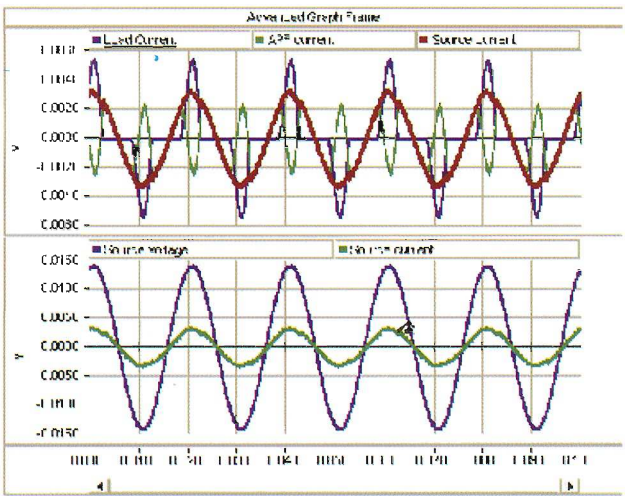
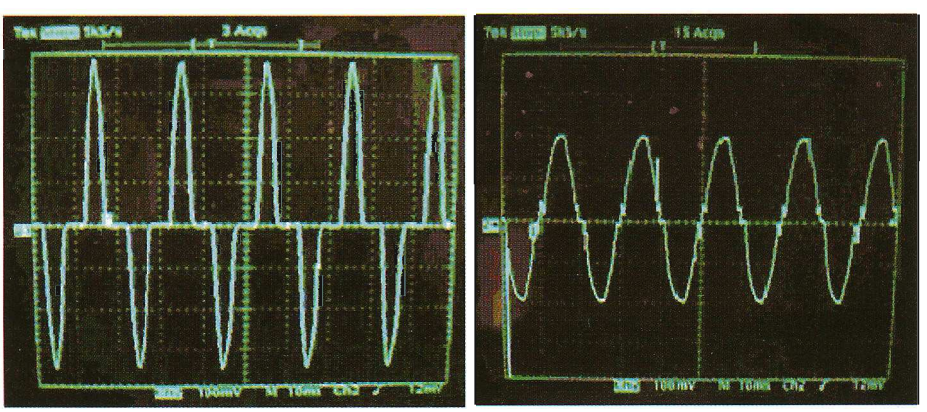


Figure 9: Source voltage and current waveforms for a bridge rectifier load with APF in operation



a) Without APF b) With APF

Figure 10: Source current waveforms with a bridge rectifier load

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